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Simulation of the Low-Power Part of Transceiving Modules of the C-Band for AESA of the MMIC Form

***V.A. Budnyaev**, engineer, VABudnyaev@sevsu.ru, Engineering Center of Micro- and Nanoelectronics Devices, Sevastopol State University, Sevastopol, Russian Federation*
***I.V. Kravchenko**, engineer, IVKravchenko@sevsu.ru, Engineering Center of Micro- and Nanoelectronics Devices, Sevastopol State University, Sevastopol, Russian Federation*
***D.A. Snegur**, postgraduate student, engineer, DASnegur@sevsu.ru, Engineering Center of Micro- and Nanoelectronics Devices, Sevastopol State University, Sevastopol, Russian Federation*
***V.V. Tumko**, engineer, VVTumko@sevsu.ru, Engineering Center of Micro- and Nanoelectronics Devices, Sevastopol State University, Sevastopol, Russian Federation*
***I.F. Filippov**, postgraduate student, engineer, IFFilippov@sevsu.ru, Engineering Center of Micro- and Nanoelectronics Devices, Sevastopol State University, Sevastopol, Russian Federation*
***V.V. Vertegel**, Cand. Sci. (Engineering), director, VVVertegel@sevsu.ru, Engineering Center of Micro- and Nanoelectronics Devices, Sevastopol State University, Sevastopol, Russian Federation*

Abstract. The paper presents the development results of electric circuits of functional units and layout of the integrated transceiver module of active electronically scanned arrays (AESA) of the C-band based on the 0.18 μm SiGe BiCMOS technology. The integrated circuit consists of control units for the amplitude and phase of a microwave signal, the reception and transmission modes switchers, amplifiers, digital control unit, and units for parameter temperature corrections. The root mean square (RMS) deviation in amplitude does not exceed 0.4 dB. The RMS deviation in phase is below 4.2 degrees. The noise factor value of the reception path does not exceed 5.2 dB. The output power in the compression point 1 dB in transmission mode is 8.5 dBm. The power consumption in the reception and transmission modes is below 195 mW and 365 mW, respectively. The layout area is 6 mm2.

Keywords: monolithic microwave integrated circuit (MMIC), transceiver module, active electronically scanned array (AESA), SiGe, BiCMOS, C-band.

Introduction

Active electronically scanned arrays (AESA) are widely used in radar systems, in radio navigation, electronic warfare, and telecommunication systems for special purposes. One of the key areas of development of domestic electronics is the increase of the production of electronic components, both dual-purpose and for civil use. AESA systems are promising in terms of their possible future implementation in fifth-generation telecommunication systems, satellite communication systems, etc. Currently, transceiving modules (TM) of the AESA are built, as a rule, based on monolithic microwave integrated circuits (MMIC) of various technology groups. The worldwide sales of MICs for AESA systems in recent years have demonstrated significant growth rates. Yet, despite the colossal functionality of such systems, they have several disadvantages. The key demerit limiting their widespread use in the civilian sector is the extremely high cost of MICs for TMs, which are manufactured primarily using GaAs-technology.

A reduction of the cost of TMs may be achieved via implementing integrated transceivers (Core Chip) that are manufactured with the use of silicon (Si) or silicon-germanium (SiGe) technologies. The implementation of the SiGe BiCMOS-technological process is capable of solving the problem of integrating the digital and analog parts of the transceiving modules, which will positively affect the final cost of the system while maintaining acceptable characteristics of TMs for civilian applications. The article presents the results of developing electric circuits and layouts of functional units of the integrated C-band TM based on 0.18 μm SiGe BiCMOS-technology. The relevance of the present study lies in the achievement of such important characteristics for AESA systems as miniaturization, stability of parameters under the influence of external climatic factors as well as reduction of series production costs.

MIC block diagram

Based on an analytical overview of mass-produced products [1–3] and literary sources [4–9] containing results of studying AESA TMs, a block diagram of an intellectual property (complex functional, IP) MIC was developed and is given in Fig. 1.

Unlike the typical block diagram of IP MIC transceiving modules, it contains a digital temperature sensor along with a correcting phase shifter and attenuator, which help to reduce the errors in setting the amplitude and signal phases conditioned by changes in temperature.

The controlled phase shifter CPS-1 and controlled attenuator CATT-1 are common units of the reception/transmission path. Switching of operation modes (reception/transmission) of the IP MIC is performed with the help of the SW-1, SW-2 and SW-3 on-off switches.

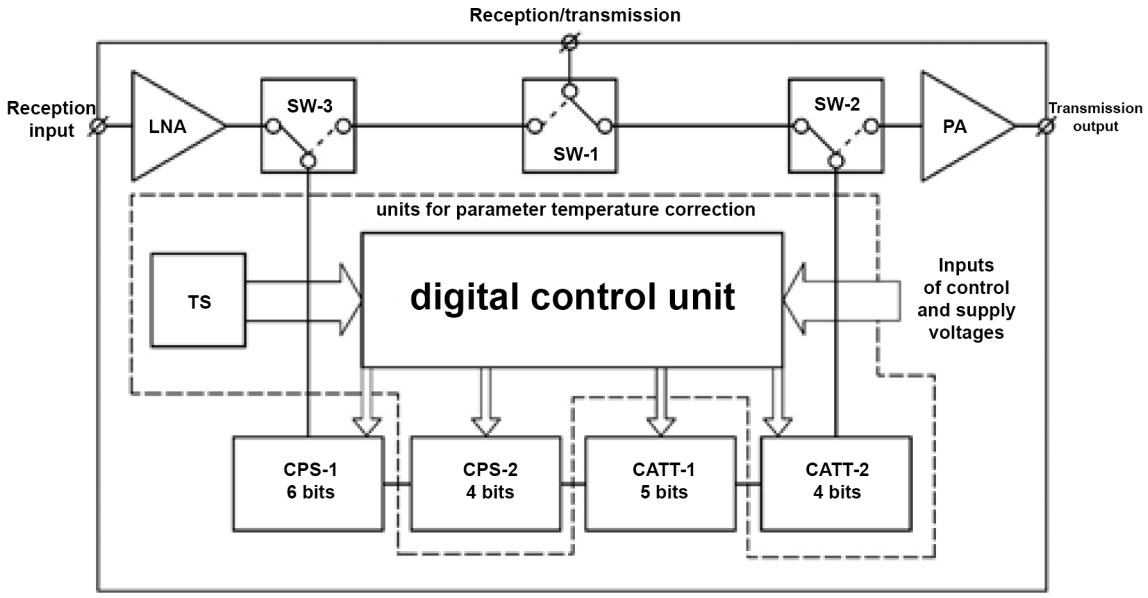


Fig. 1. IP MIC block diagram.

The low-noise amplifier (LNA) ensures an increase in the signal level at the input of the reception path to the required values, having the lowest possible value of the noise factor. The power amplifier (PA) provides the required level of the microwave signal at the output of the transmission path.

The integrated temperature sensor (TS) generates a temperature-dependent voltage and converts it into digital codes. Based on these codes, the digital control unit (DCU) corrects the phase shift and attenuation with the use of the CPS-2 phase shifter and CATT-2 attenuator. For data exchange between the IP MIC and the control microcontroller, a serial peripheral interface is included into the DCU. With the help of external digital signals, the DCU ensures switching between operation modes, controls the parameters of the CPS-1 phase shifter and CATT-1 attenuator.

The block diagram does not show the functional unit of the reference voltage source (RVS), with the help of which the given operation mode is ensured by the direct current of all of the units of the IP MIC.

MIC functional nodes and their characteristics

Low-noise amplifier

A simplified electrical diagram of the LNA is given in Fig. 2.

The VT1 transistor is connected with the common base in the circuit for ensuring coordination of the input impedance of the first stage of the LNA with a resistance of 50 Ω in a wide bandwidth. A cascode amplifier based on VT2 and VT3 field-effect transistors, due to the partial elimination of the influence of the Miller effect, has a high voltage gain without narrowing the operating frequency band. The low-pass filter in the base circuit of the transistor VT1 is necessary to prevent the ac component of the voltage from entering the output of the reference voltage source. Thus, stabilization of the operating point of the VT1 transistor, as well as the reduction of the noise factor of the stage are achieved.

Figures 3 – 4 give the results of LNA general circuit simulation with account for parasitic elements of the layout.

The gain in the frequency range 4– 6 GHz is 21-22 dB and the noise factor does not exceed 4.7 dB. The value of the return losses at the input in the operating frequency range exceeds 15 dB.

The compression point of 1 dB at the input (IP_{1dB}) in the operating frequency range exceeds 22 dBm. The input third-order intermodulation intercept point (IIP3) is at least 12 dBm.

Controlled phase shifter

The CPS-1 includes (Fig. 5):

- a balancing device (BD; balancer), which performs the conversion of an asymmetric input signal into a symmetric (balanced) output signal;

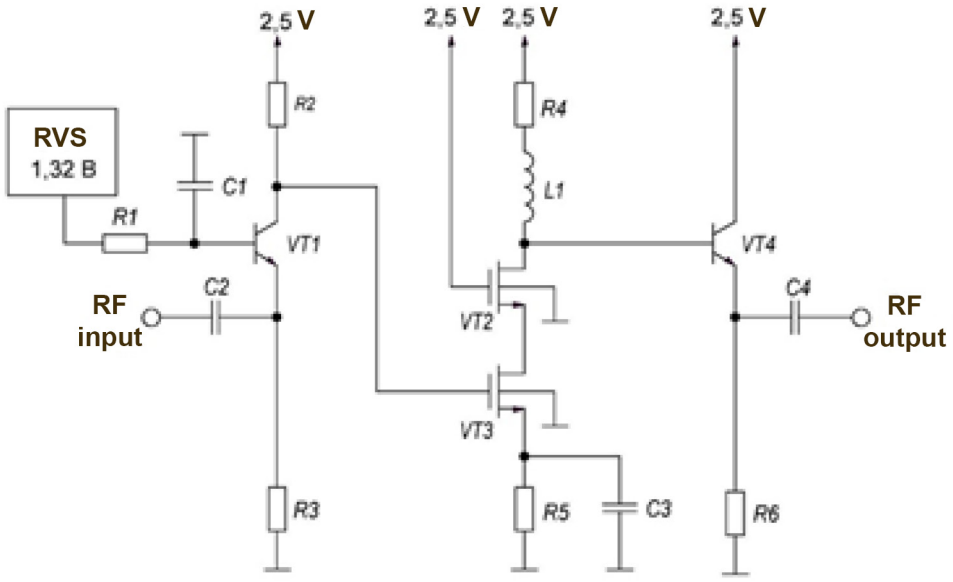


Fig. 2. Electric circuit of the LNA.

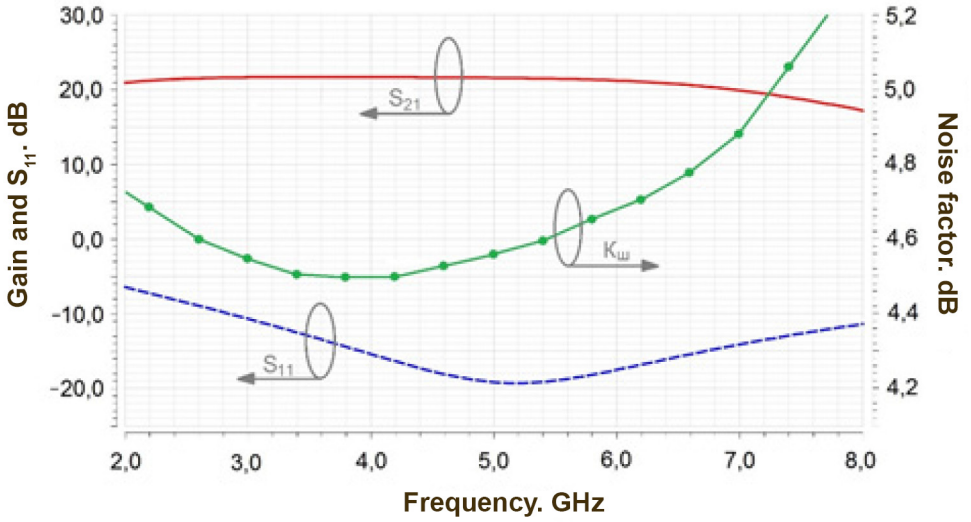


Fig. 3. Frequency dependences of small-signal LNA parameters.

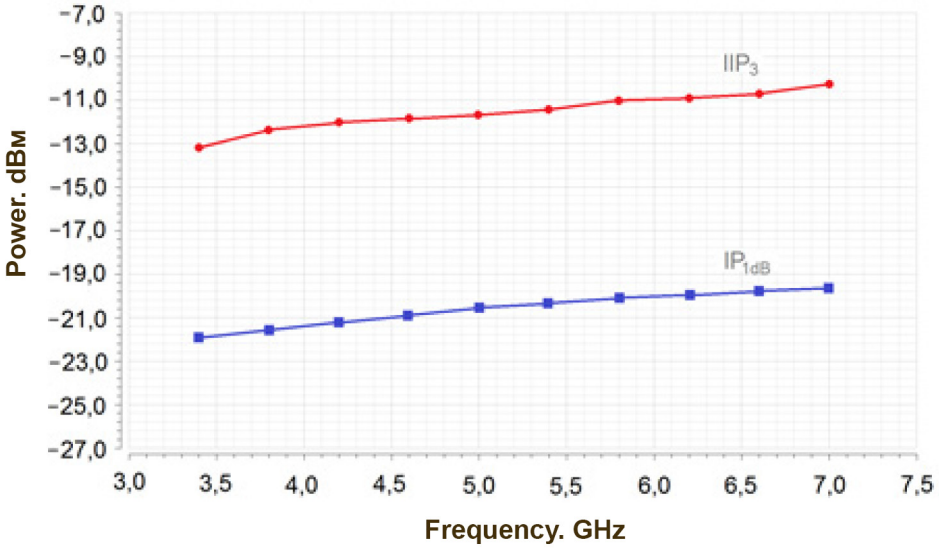


Fig. 4. Dependence of IP_{1dB} and IIP_3 on the frequency.

- a polyphase filter (PPF), which divides the balanced signal into orthogonal components;
- a dual adder based on Gilbert cells (DA) responsible for the weighted summation of the components;
- a controlled attenuator (ATT);
- a current digital-to-analog converter (DAC), which is a circuit of the driver of analog control signals by an adder (summator);
- a buffer amplifier (BA) at the output of the circuit, which is necessary for the compensation of the attenuation introduced by the indicated CPS-1.

The key feature of the given phase shifter is the implementation of an additional stage of a controlled attenuator, which allows reducing the amplitude error introduced when switching phase samples. The use of frequency and temperature–dependent feedback allows us to adjust the amplitude-frequency and temperature characteristics of the phase shifter.

The adder and attenuator are controlled simultaneously using circuits of current DACs, which are a binary current matrix controlled by transistors in key mode. Furthermore, the inputs of every current DAC are connected in parallel. Thus, the adjustment (correction) does not require additional control bits [10]. Fig. 6 demonstrates the frequency dependences of the transmission factor and phase states of the CPS-1 when switching phase samples.

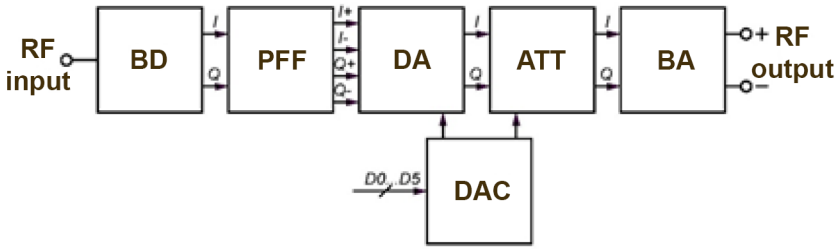
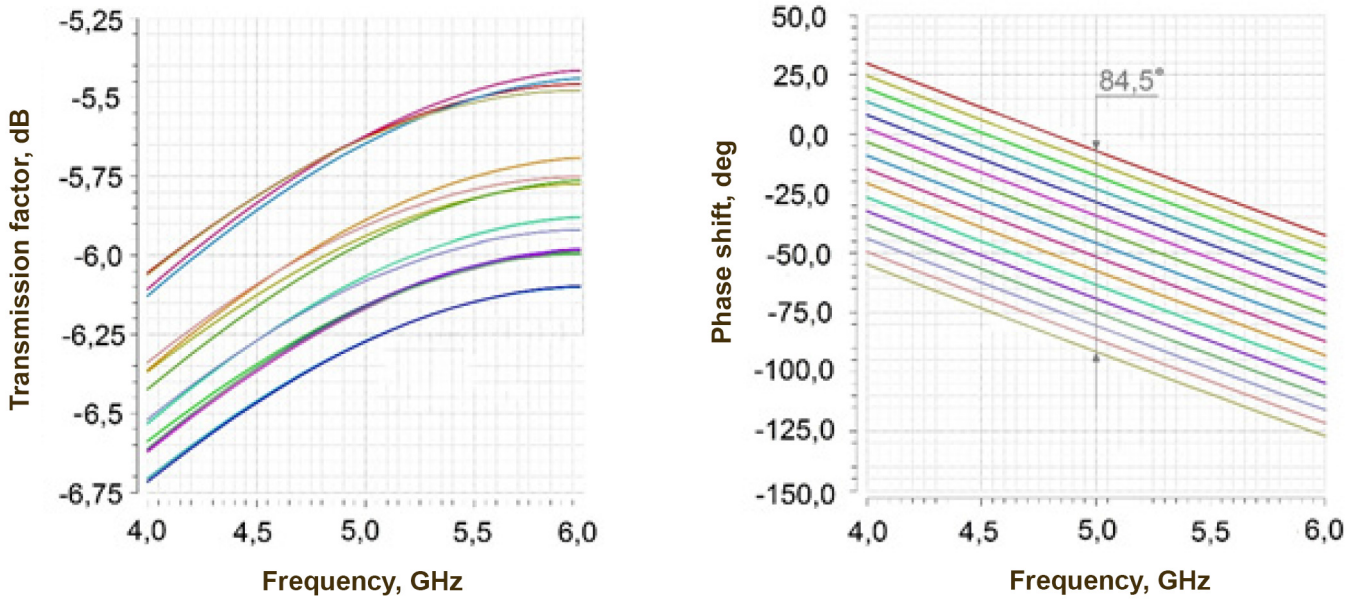


Fig. 5. CPS-1 block diagram.



a) b)

Fig. 6. Amplitude (a) and phase (b) frequency characteristics of the CPS-1 during phase adjustment within one quadrant.

Table 1. Parameters of the developed phase shifters

Parameter, unit	CPS-1	CPS-2
Range of operating frequencies, GHz	4—6	
Range of operating temperatures, °C	–60—85	
Range of phase adjustment, deg	360	8
Adjustment step size, deg	5.625	0.5
Phase-setting error, deg	<1.005	<0.25
Transmission factor, dB	–6	5.9
Amplitude error, dB	<0.703	<0.1
Supply voltage, V	2.5; 5	2.5; 5
Current consumption, mA	<35	<27

The circuit of the correcting phase shifter CPS-2 is analogous to the circuit of the main CPS-1. The correcting phase shifter does not include a controlled attenuator circuit, since it has a relatively small value of the amplitude error within the limit of the range of operating frequencies and temperatures.

The key parameters of the phase shifter obtained as a result of their simulation are set forth in Table 1.

Controlled attenuator

When developing an IP MIC based on silicon-germanium technologies for controlling the amplitude of the output signal, it is reasonable to use an active controlled attenuator (amplifier with a variable transmission factor) because it has a relatively low amplitude error, permits to eliminate the insertion losses and occupies a relatively small area on the chip. The block diagram of the developed CATT-1 is given in Fig. 7.

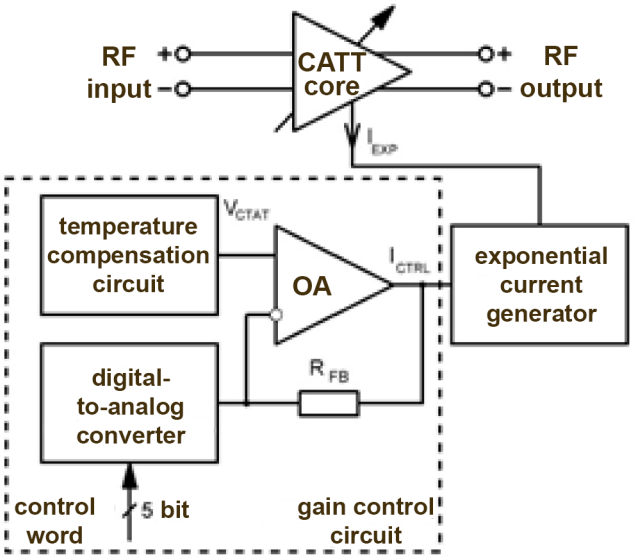


Fig. 7. CATT-1 block diagram.

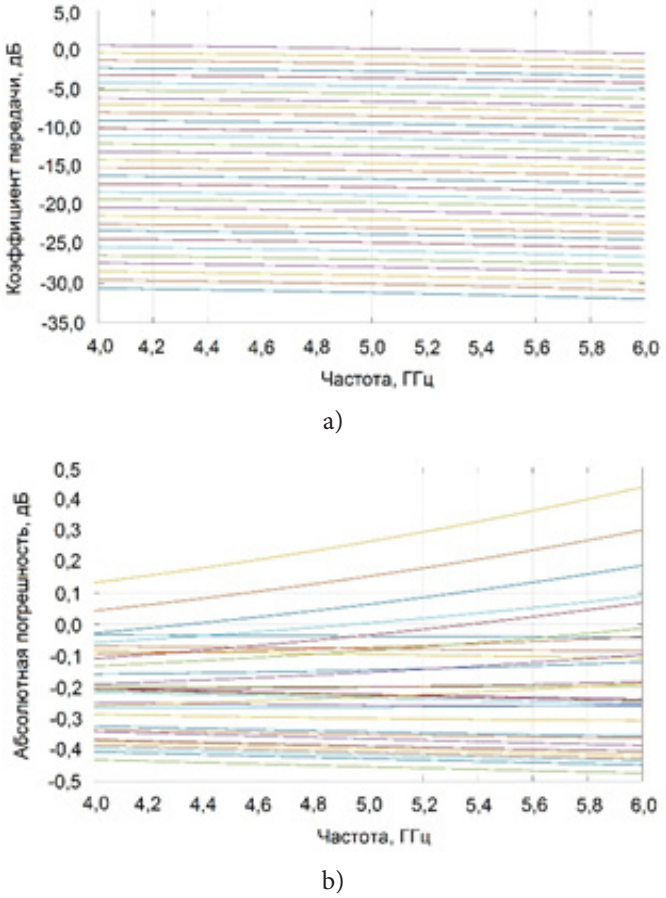


Fig. 8. Frequency dependences of the transmission factor (a) and the absolute amplitude error (b) of CATT-1.

The key element of the circuit is the CATT core, which changes the amplitude of the differential microwave signal at the input of the attenuator. The core consists of a classic differential stage with a pair of oppositely connected transistors with "a floating emitter" [11]. Such a connection allows us to widen the adjustment range of the attenuation factor of the circuit. Emitter followers are implemented at the output of the circuit in order to match the CATT-1 with the next stage of TMs.

To ensure a uniform step size in changing the transmission factor of the attenuator, a nonlinear current generator, which uses an exponential form of the transmission characteristic of the bipolar transistor, is introduced.

The control circuit generates the control signal for the exponential current generator and includes the DAC, a temperature compensation circuit and an operational amplifier (OA). The voltage at the output of the temperature compensation circuit is inversely proportional to the temperature (V_{STAT}), which allows us to compensate the increase in the current via the differential stage of the core and ensure the temperature stability of the attenuator. In Fig. 8a, the frequency dependences of the attenuator gain are presented for various states of the control code (from 0 to 31). Fig. 8b shows the frequency dependences of the absolute error of the attenuator.

The range of variation of the transmission factor is 31.3 dB on the central frequency of 5 GHz. In this case, the non-uniformity of the transmission factor at maximum attenuation is 1.8 dB and at minimum – is 1.08 dB. Across the entire range of operating frequencies, the absolute error of setting the transmission factor does not exceed 0.48 dB and the root mean square deviation is 0.178 dB.

The functional unit of the correcting CATT-2, in terms of the general circuit solution, copies the main CATT-1. The difference lies in the magnitude of the reference currents of the DAC. In the DAC of the CATT-2, they are reduced in order to obtain a smaller adjustment range of the circuit transmission factor. The main parameters of the developed main and correcting attenuators are given in Table 2.

Microwave switch

In the developed circuit of a single-pole switch in two directions (Fig. 9), to increase the isolation, parallel switching of shunt field-effect transistors is used.

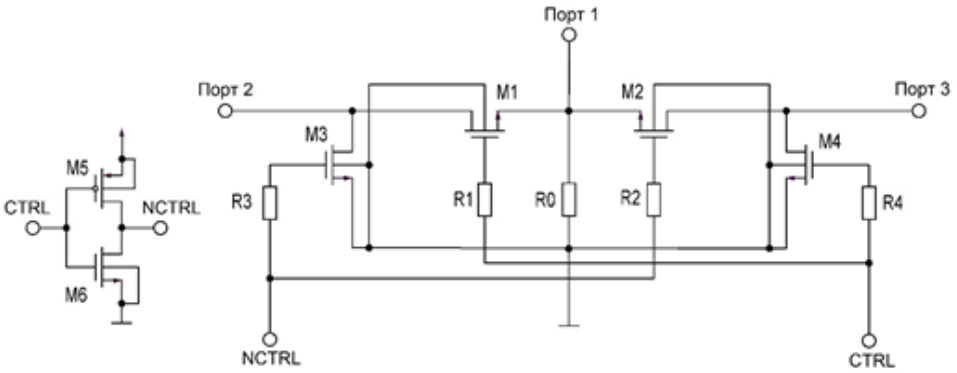
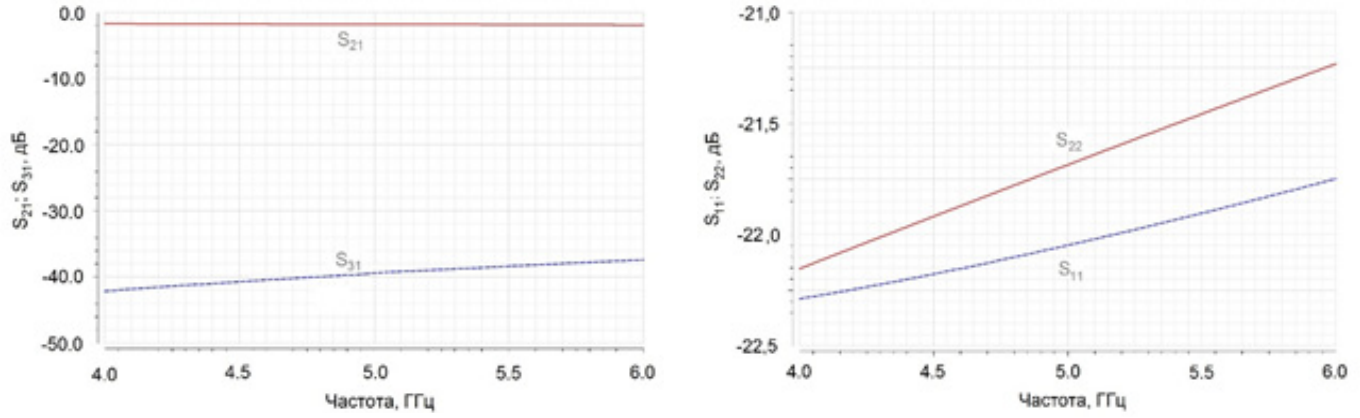


Fig. 9. Electric circuit of the microwave switch.



a) b)

Fig. 10. Frequency dependences of parameters S_{21}, S_{31} (a) and S_{11}, S_{22} (b) of microwave switches.

Table 2. Parameters of the developed attenuators

Parameter, unit	CATT-1	CATT-2
Range of operating frequencies, GHz	4—6	
Operating temperature range, °C	–60—85	
Range of insertion losses, dB	–31—0	–3.56—0.21
Attenuation step size, dB	1	0.25
Amplitude error, dB	<0.48	<0.028
Phase error, deg.	<5.3	<0.37
Compression point of 1 dB at output, dBm	–30	–27
HDF at max. signal amplitude, %	0.72	0.8
Noise factor, dB	<18	
Supply voltage, V	2.5; 5	
Power consumption, mW	17.3	15.45
Footprint, mm^2	0.009	

The M1 and M4 transistors are controlled in-phase by the CTRL voltage; the NCTRL voltage controls transistors M2 and M3. Thus, when the M4 is in the ON-state, the part of the signal, which passed the closed M2 transistor, is shunted to the ground. In the other channel of the switch, the M3 transistor will be in the OFF-state and practically will not affect signal passage. The M5 and M6 transistors generate an inverse control signal for the NCTRL.

The transmission characteristics of the open (S21) and closed (S31) channels of the switch are given in Fig. 10a. Insertion losses in the operating frequency band do not exceed 1.9 dB, and isolation is more than 37 dB. The return losses at the input and output exceed 21 dB (Fig. 10b).

Power amplifier

A simplified electric circuit of the power amplifier (PA) is given in Fig. 11. The PA provides the required signal power level at the input of the IP MIC under development with a minimal level of non-linear distortions.

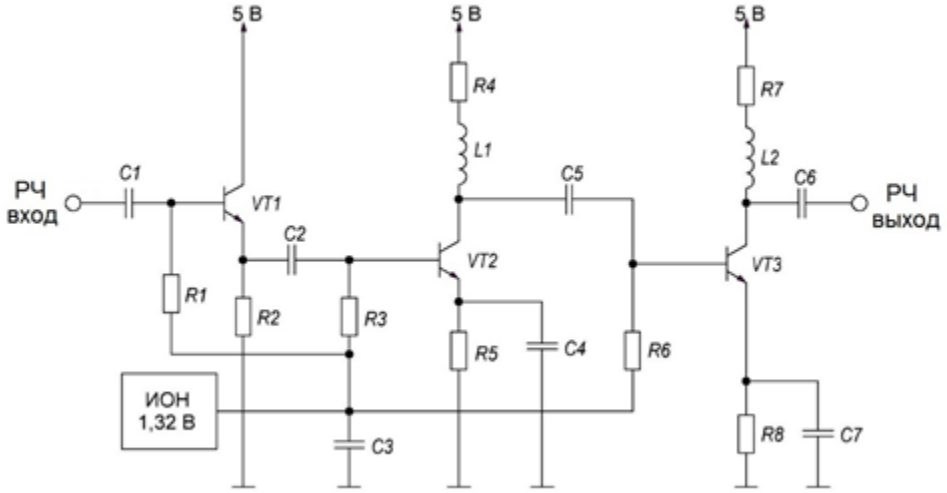


Fig. 11. PA electric circuit.

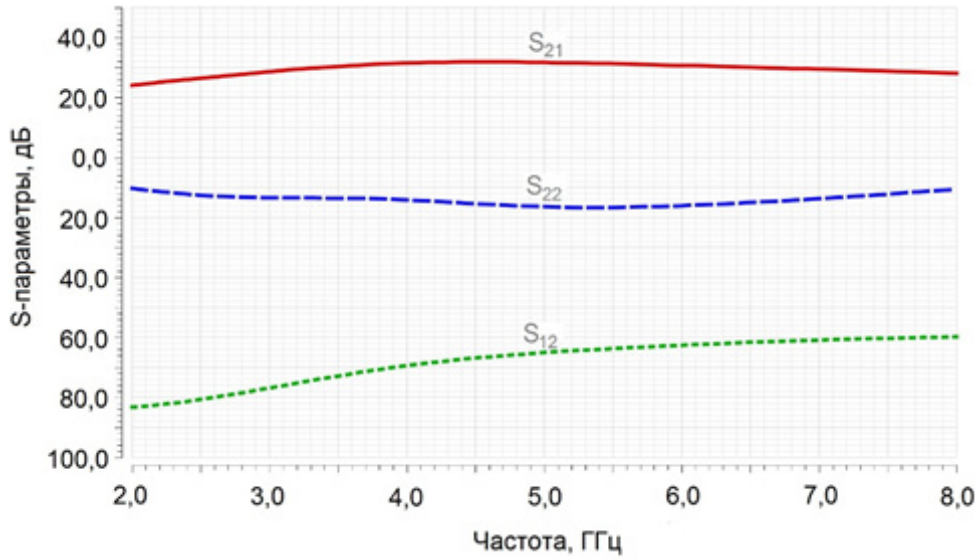


Fig. 12. Frequency dependences of low-signal parameters of PA.

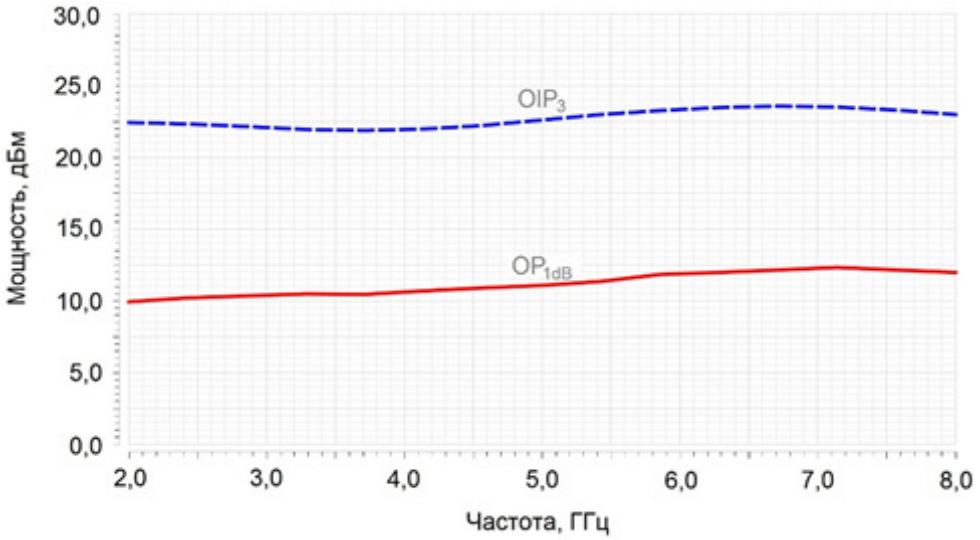


Fig. 13. Dependence of OP_{1dB} and OIP_3 of the PA on the frequency.

The first stage in the circuit with a common collector ensures the coordination of the input impedance of the PA with the output impedance of the previous stage. The second and third stages in the circuit with a common emitter provide the necessary value of the gain. The bias voltage of the VT1–VT3 transistors is 1.3 V and is set with the help of the RVS. For stabilizing the operating points of the transistors and preventing the alternating current component of the voltage from reaching the RVS output, elements R1, R3, R6 and C3 are employed.

The amplifier ensures a gain of 26.5–28 dB in the 4–6 GHz frequency range. Return losses at the output exceed 13 dB (Fig. 12).

Fig. 13 demonstrates the dependences of the 1 dB output compression point (OP_{1dB}) and the point of intersection of the 3rd order output intermodulation (OIP_3) on the frequency. The consumed power from the power supply with a voltage of 5 V is 295 mW.

Dependences of the harmonic distortion factor (HDF) and the energy conversion efficiency of added power (ECE_{AP}) at the input power level are presented in Fig. 14. At a PA input power level of 17.6 dBm (compression point of 1 dB at the input), the HDF is 5.8%, and the ECE_{AP} ¾ 5.6%.

Temperature sensor

The integrated temperature sensor (TS) includes three functional units: a temperature sensor, an analog-to-digital converter and a voltage regulator. The sensor uses the principle of first-order compensation, which involves the summation of temperature factors of the

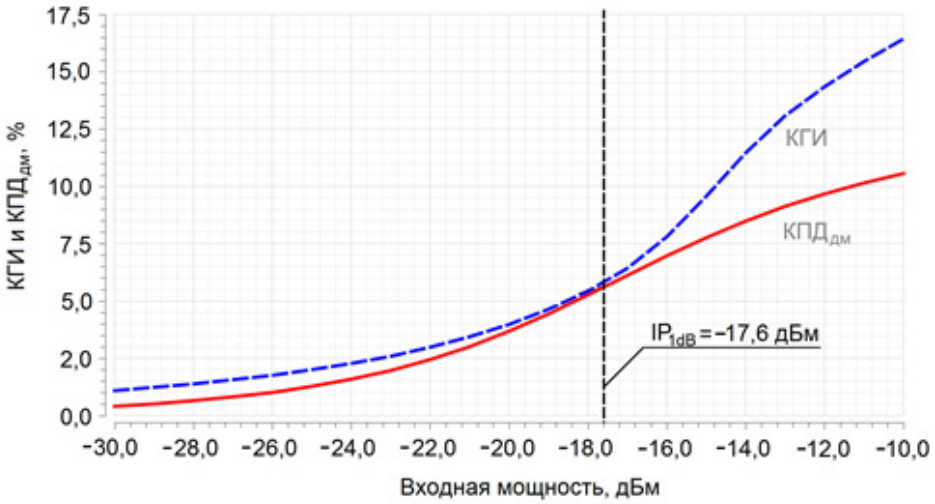


Fig. 14. Dependence of HDF and ECE_{AP} on the input power level.

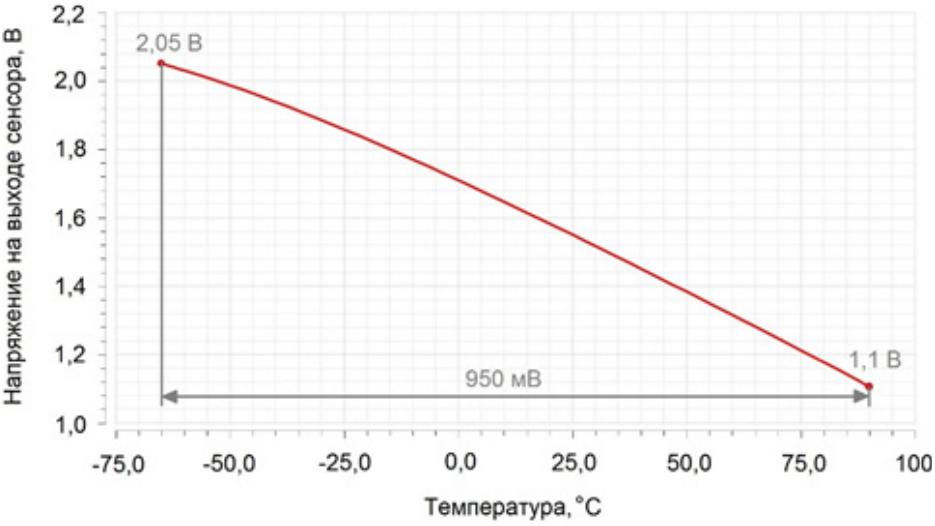


Fig. 15. Dependence of the output voltage of the sensor.

resistance of the p-n junction of the bipolar transistor with the temperature factors of additional transistors. The sensor circuit includes a pair of bipolar transistors, which are controlled by the voltage at the output of the divider formed by resistors selected in such way that the voltage at the collector of one of the transistors depends on the temperature as much as possible (Fig. 15).

In order to provide power for the temperature sensor, a stabilizer based on an operational amplifier with feedback is used. This stabilizer generates a voltage of 2.51 V at its output when the supply voltage changes in the range from 4.5 to 5.5 V. The output voltage of the stabilizer weakly depends on the temperature of the chip. The temperature dependence of the output voltage of the sensor is converted into a parallel digital code with the help of a counter-type analog-to-digital converter. The results of sensor simulation are set forth in Table 3.

Table 3. Parameters of the integrated TS

Parameter, unit	Value
Range of measured temperatures, °C	–65—90
Bit depth of the sensor, bit	5
Resolution, °C	5.156
Measurement error, °C	<5
Measurement time, μs	<1 ($f_{cl.f.}$=50 MHz)
Consumption current, mA	6
Layout area, mm^2	0.025

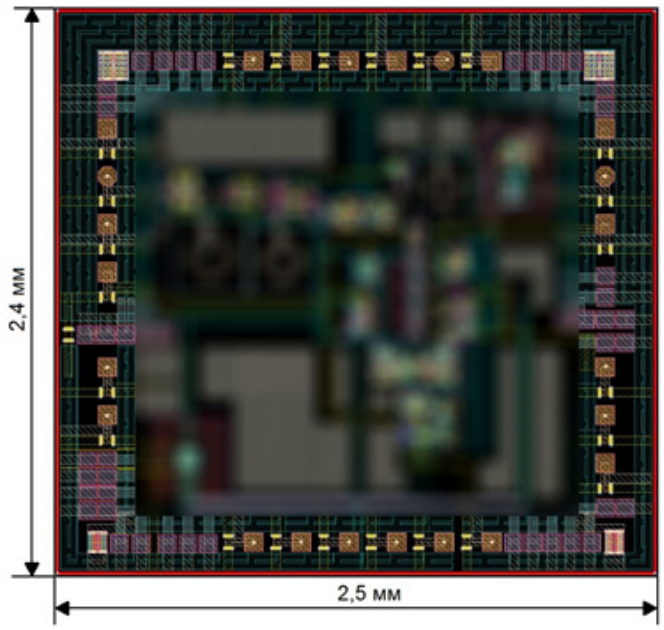


Fig. 16. IP MIC layout.

Result of IP MIC simulation

Fig. 16 presents the developed layout of the IP MIC. The linear dimensions of the layout are 2.5×2.4 mm. The layout area is 6 mm^2.

The IP MIC characteristics that were obtained with the help of circuit simulation with account for parasitic elements of the layout are given in Table 4. The chosen approaches to the design, circuit and layout solutions, as well as the stability of the technological process allows us to count on a satisfactory result after the production of a test batch of IP MICs [12,13].

Table 4. IP MIC parameters

Parameters, unit	IP MIC under development	
	Reception mode	Transmission mode
Range of operating frequencies, GHz	4—6	
Range of operating temperatures, °C	–65—85	
CPS-1 bit depth, bit	6	
CPS-1 least significant bit, deg	5.625	
CATT-1 bit depth, bit	5	
CATT-1 least significant bit, dB	1	
RMS deviation in phase, deg	<4.2	
RMS deviation in amplitude, dB	<0.4	
Transmission factor at a frequency of 5 GHz, dB	35	33
Non-uniformity of the transmission factor in the operating frequency band, dB	<1.9	<3.5
Upper limit of output linearity, dBм	–19.7	8.5
Noise factor at a frequency of 5 GHz, dB	<5.2	—
VSWR in output, units.	<1.8	<1.3
VSWR in input, units	<1.33	<1.8
Isolation between reception and transmission channels, dB	>50.5	>62.5
Bit depth of the control code of the DCU, bit	19	
“0”/“1” of the DCU, V	0/1.8	
Supply voltage, V	2.5; 5	
Consumption current, mA	<39	<73
Power consumption, mW	<195	<365
Layout area, mm^2	6	

Conclusion

The article sets forth the results of developing an IP MIC transceiving module of a C-band AESA. The integrated circuit contains one reception/transmission channel. Switching between operating modes of the IP MIC is performed by changing the state of microwave switches. The amplitude and output signal phase are controlled by changing the state of the controlled phase shifter and attenuator. The implementation of a circuit for the correction of IP MIC parameters based on an integrated TS, correcting CPS-2 и CATT-2 allows ensuring the stability of the parameters of the transceiving module in a wide range of operating temperatures. The noise factor in reception mode does not exceed 5.2 dB. The 1 dB compression point in output in transmission mode is 8.5 dB. The power consumed in reception and transmission modes does not exceed 195 mW and 365 mW, respectively. Considering the obtained characteristics, the IP MIC can be widely implemented as part of a low-power base station of fifth-generation telecommunication systems.

Sources of financing

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