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A Method of Detecting of Internal Defects of CMOS-Microcircuits

I.Yu. Bulaev, *bulaev.ivan@gmail.com*
Joint Stock Company "Russian Space Systems", Moscow, Russian Federation

Abstract. For the acquisition of highly reliable equipment it is necessary to allow only those electronic components, which before the installation phase are fully functional and parametric. The testing center is often not able to conduct a full-fledged functional control of the electronic components products, because does not have information about internal blocks of complex functional products and how they interact with each other. The situation is complicated by the fact that the degree of integration and functionality of modern microcircuits is constantly growing. Another problem is the forecasting of further trouble-free operation of the product and the detection of internal hidden defects. At an early stage of operation, the microcircuit can contain insignificant internal hidden defects, the value of which practically does not affect the performance of the microcircuit. However, after a certain amount of time has elapsed as a result of the degradation processes of the product materials, the defect may increase and lead to irreversible failure of the product. Therefore, it is extremely important at the stage of autonomous testing of a product, not as part of equipment, to detect such internal defects. The article explains the need to search for small hidden defects in ECB products, suggests comparison of the most popular diagnostic methods, discusses the problems of using existing methods for diagnosing modern microcircuits, suggests an approach to detecting small internal defects of the microcircuit before the stage of its installation in equipment.

Keywords: defect, failure, CMOS, diagnostics, tests

Internal defects of electrical, electronic and electromechanical (EEE) parts, which include diodes, transistors, integrated microcircuits, microassemblies, passive components, etc., can sometimes not be detected by ordinary functional or parametric control. In cases where the defects are too small, they do not have a significant effect on the operation of the EEE products (hereinafter - the products) and do not lead to either the falling of electrical parameters beyond the permissible norms, or to a malfunction.

However, after a certain amount of time has elapsed as a result of the degradation processes of the product materials, the defects may increase in magnitude and lead to irreversible failure of the product. Therefore, it is extremely important at the stage of off-line testing of a product, not as a part of equipment, to detect such internal defects.

In addition, the complexity of modern microcircuits is so great that the task of performing full functional control of all internal components "in the far corners" of the product becomes practically impossible. The situation is aggravated by the fact that the tester, as a rule, does not have any information about the internal structure and circuitry implementation of the microchip.

To identify hidden defects and compensate for insufficient functional monitoring, such methods as burn-in testing are used, during which the products are influenced by various factors that accelerate the aging process of materials: voltage, temperature, etc. With such testing, within a relatively short time period (several days), it is possible to simulate a certain lifetime of the product (several years). After the test, either the potentially unreliable products fail, or the drift of their informative parameters (the difference in valuesmeasured before and after burn-in testing) will be very different from the drift of serviceable products.

However, burn-in testing is a fairly long and expensive test, requiring specialized equipment, rigging and method selection techniques. Burn-in testing methods can be replaced by diagnostic non-destructive testing (NDT) methods, which indirectly, by measuring electrical parameters (currents, voltages, time intervals), judge whether there are internal defects in the product.

Practically all methods of NDT are based on statistical processing and comparison of the measured parameters for a batch of products under the same impact. NDT applicable only for products of the same batch.

Hereafter, products containing a defect will be referred to as "unreliable", and the products not containing a defect will be referred to as "reliable".

NDT methods, in addition to their advantages, which include the ability to reject unreliable products at minimal cost, have a number of disadvantages.

It should be noted that not all of the above methods are applicable to any type of EEE products. Table 1 demonstrates the applicability of NDT methods for each type of EEE product.

From the table it is seen that for the NDT of microcircuits and microassemblies all the above methods are applicable, while for the control of the passive components there are the fewest methods. On the one hand, this situation seems logical; microcircuits and microassemblies are the most complex types of EEE products, and to verify their quality, it is necessary to conduct as many inspections as possible. On the other hand, from the conclusions of the commissions on the analysis of failures of devices it is evident that often the cause of the malfunction is a hidden defect in one of the passive components.

Thus, it is necessary to conduct research on the development of new, more advanced NDT techniques for passive components.

Table 2 shows the advantages and disadvantages of NDT methods.

A common disadvantage of NDT methods is that in the case of a defect in most products in the batch, there is a risk of rejecting of reliable products, because their parameters may not fall into the confidence range, while unreliable products will not be rejected at all. The main reason for this problem lies in the absence of a "reference" sample with previously unknown culling boundaries, whereby it is necessary to determine the boundaries using statistical methods.

To solve this problem, it is proposed to organize the cooperation of manufacturers of EEE products with test centers, which should consist in transferring to the testing centers of the models on which it would be possible to assess the degree of change in the parameters of the product when a defect of a certain value is introduced into one or another part of the product.

In addition, it follows from the table that a number of methods require the use of high-precision measuring equipment and sophisticated testing equipment, which is practically absent from the Russian market. The use of foreign-made equipment entails certain problems related

Table 1. Applicability of NDT methods for different types of EEE products

Type of method	Integrated microcircuits and microassemblies	Semiconductor devices	Passive components
Tightened norms	+	+	+
Static current consumption	+	-	-
Dynamic current consumption	+	-	-
Critical power supply voltage	+	-	-
Hysteresis of the parameters	+	+	+
Current-voltage analysis	+	+	-
Radiation methods	+	+	+
Low frequency noise	+	+	+
Electrostatic method	+	+	+

Table 2. Advantages and disadvantages of different NDT methods.

Type of method	Advantages	Disadvantages
Tightened norms	A method simple in the implementation that allows detecting products with anomalous characteristics	Danger of rejecting the reliable samples
Static current consumption	A method simple in the implementation that allows detecting internal parasitic resistances	It is impossible to detect small defects in products with a high degree of integration
Dynamic current consumption	A method that makes it possible to detect internal parasitic resistances and capacitances	High complexity of implementation and processing of results
Critical power supply voltage	A method simple in the implementation that allows detecting internal parasitic resistances	None
Hysteresis of the parameters	The ability to detect products with unstable construction	Requires high-precision measuring equipment and expensive test equipment
Current-voltage analysis	The possibility of detecting defects of *p*-*n*-junctions	There is no possibility to diagnose *p*-*n*-junctions of internal gates of microcircuits
Radiation methods	Detection of objects with reduced resistance to radiation	High complexity of implementation, risk of damage to the product
Low frequency noise	Detection of samples with an increased number of impurities, dislocations and microfissures	High-precision measuring equipment is required
Electrostatic method	Detection of objects with reduced resistance to electrostatic discharge	High complexity of implementation, risk of damage to the product

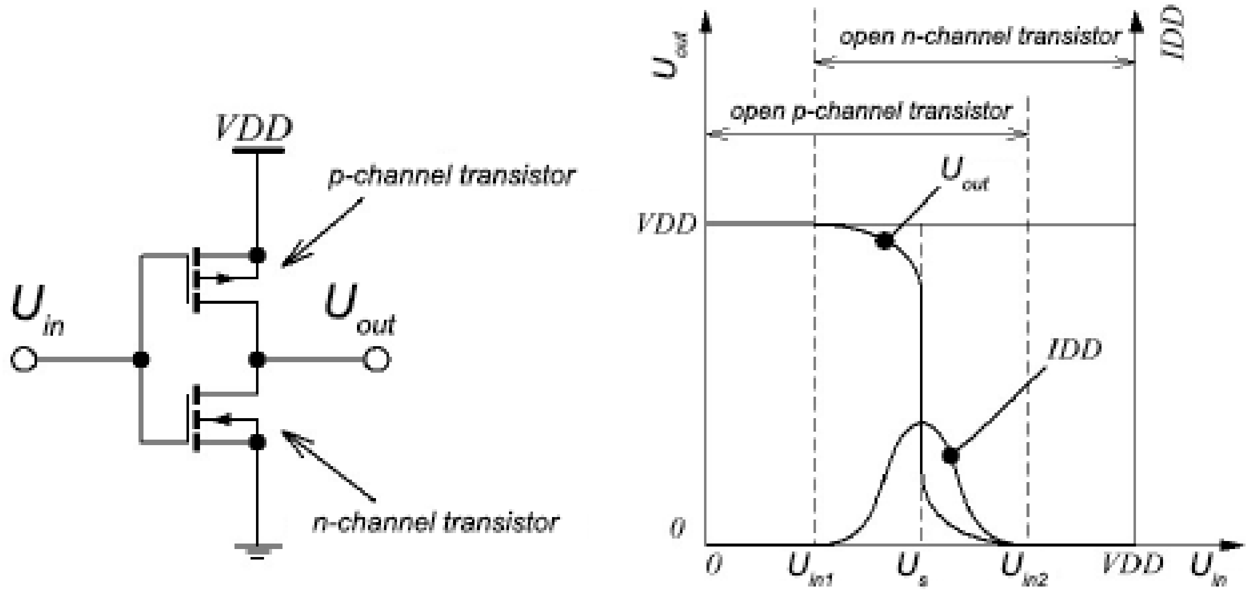
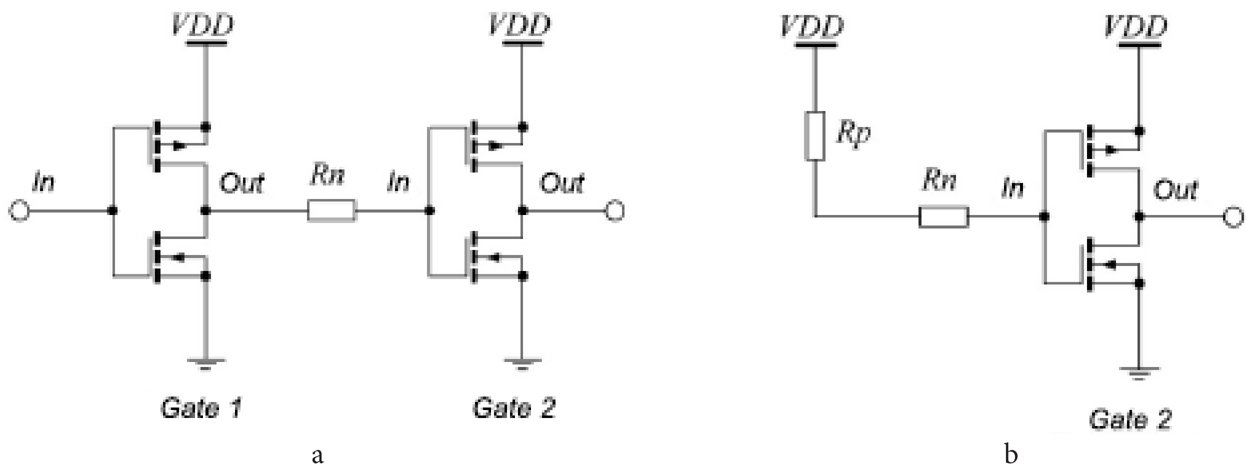


Fig. 1. CMOS inverter transfer characteristic



a b

Fig. 2. The connection of the two gates through the parasitic resistance *Rn* (a) and the equivalent circuit with the voltage at the input of the first gate equal to 0 V (b)

to the cost, delivery times and the level of technical support. To solve this problem, it is necessary to develop own equipment that can provide the necessary level of accuracy and effects.

A major problem is that, due to the increased integration of modern EEE products and the use of fundamentally new materials, the old NDT methods show low efficiency and their use in the testing process is not economically viable. lt is necessary to carry out work, involving test centers and manufacturers of EEE parts, to improve the old methods and develop new ones. The work should include mandatory testing of the effectiveness of NDT methods, for example, by performing a correlation analysis of NDT results and resource tests.

In addition, correlative analysis of NDT and burn-in testing results should be carried out. In the case of obtaining a high correlation, it is necessary to replace the long-term and expensive burn-in testing with NDT.

At the moment, the EEE manufacturers do not recognize the results of the NDT carried out at a testing center. This leads to the fact that the customer of the tests does not have the opportunity to carry out the complaint work for products rejected by the results of NDT. To solve this problem, it is proposed to approve some NDT methods at the level of state or industry standards.

The most widely used NDT methods, such as rejection for static and dynamic consumption currents,

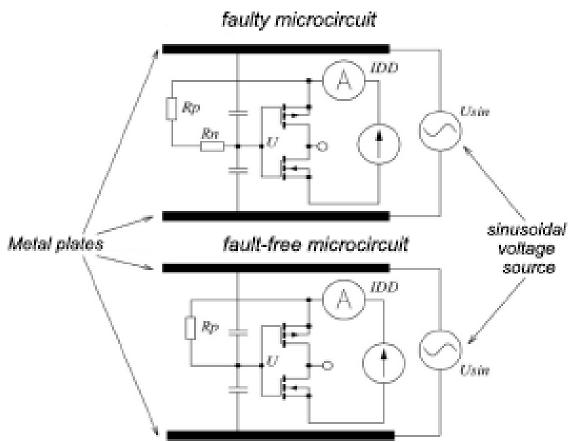
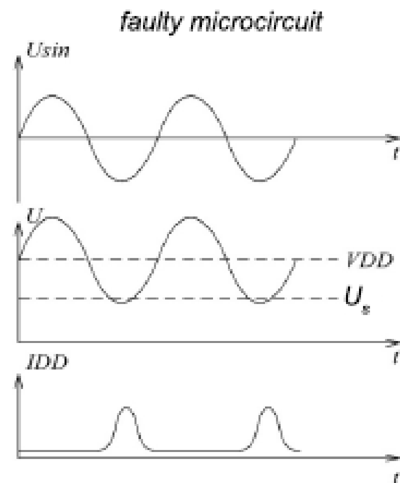


Fig. 3. Scheme of the experiment



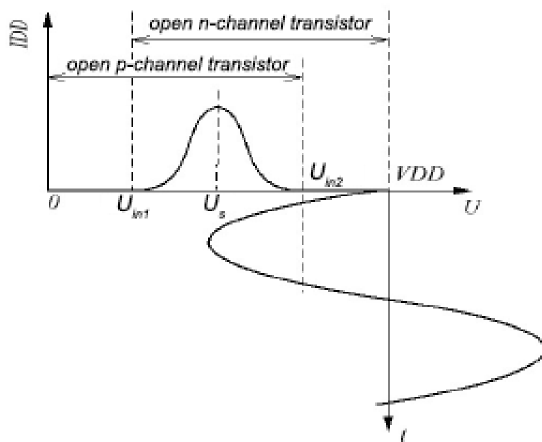


Fig. 4. The appearance of the pulse of the *IDD* current consumption during interference at the input of the gate *U* of the threshold value U_t

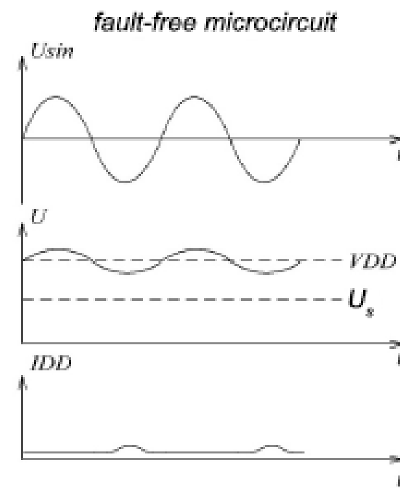


Fig. 5. The difference in the oscillograms of the current consumption of *IDD* in a fault free and faulty microcircuit with the same voltage level *Usin*

critical supply voltages, etc., have one common drawback: in order to detect a defect, it must be "activated", i.e. switching a gate containing a defect from one logical state to another. Thus, to ensure 100% test coverage, it is necessary to switch each gate of the EEE product and at the same time make an informative parameter measurement, which is difficult for modern microcircuits. Therefore, there is a need to develop NDT methods that affect the entire product in an integrated manner and detect the presence of a defect anywhere in the structure of the product, albeit without the possibility of its localization.

The most common internal defects of modern CMOS chips are low resistance (in the extreme case, a short circuit) between two points of the circuit where the resistance should be maximum, or a large resistance (in the extreme case, an open) between two points where resistance should be minimal. In foreign literature, such defects are called "short" and "open" [1].

If the defect of the microcircuit is minor (for example, closing the output of the gate to 10 kΩ or an incomplete opening of the conductor between two gates, increasing the resistance of the circuit by 100 Ω, etc.), it may not be detected during routine functional and parametric control because of the imperfection of the tests and characteristics of control and measuring equipment.

However, when such a chip will work for some time as a part of equipment, the proportions of the defects may increase, which will lead to the failure of the chip. Thus, it is necessary to detect such defects before the installation of the chip into the equipment. The problems of detecting

defects of the "short" type were discussed in [2]. This article provides a theoretical justification for the method of searching for defects of the "open" type.

Consider the transfer characteristic of a CMOS gate (Figure 1). With the voltage at the input of the gate *Uin* from 0 V to *Uin1*, the n-channel transistor is closed, the p-channel transistor is open; there is no connection between the power supply and the ground of the chip and the *IDD* consumption current is practically zero. A similar situation occurs when the voltage at the gate input is in the range from *Uin2* to *VDD*, when the *p*-channel transistor is closed and the *n*-channel transistor is open. With the voltage at the gate input in the range from *Uin1* to *Uin2*, both transistors open, forming a galvanic connection between power and ground. In this case, the current consumption of the chip increases, and the maximum it will be at the voltage at the input of the gate equal to the threshold switching voltage *Us*.

Defects of the "open" type in CMOS structures are divided into two main types: a gate opening and a drain or source opening. Consider the first type: the appearance of parasitic resistance *Rn* between the output of the first gate and the input of the second gate (Figure 2, a). Suppose that the input of the first gate is set to 0 V. Then the output of the first gate connects the input of the second gate to the power supply through the series resistance of its p-channel transistor Rp *and the parasitic resistance* Rn *(Fig. 2b).*

Thus, in comparison with a fault free microcircuit, in a defective chip, the gate input has a weaker connection with the power supply, and, therefore, is more susceptible to interference effects.

We place the microcircuit in an alternating electric field, placing it between two metal plates to which a sinusoidal voltage is applied, and we will make a measurement of the current consumption (Figure 3). Between each point of the chip and the metal plates, a capacitance is formed, therefore, the inputs of all the gates of the chip will be interfered with, the magnitude of which can be varied by the amplitude and frequency of the sinusoidal voltage.

The level of induced interference *U* at the input of the gate of the faulty chip will be greater than that of the fault free one. By increasing the amplitude and frequency of the sinusoidal voltage *Usin*, one can achieve a level of interference sufficient to open the p-channel transistor (Fig. 4).

In this case, the through consumption current will flow. For a working chip with the same sinusoidal voltage parameters, the interference level will be much lower and will not lead to gate switching (Fig. 5).

Thus, by varying the parameters of the sinusoidal signal and comparing the consumption currents of individual samples of a single batch of chips, it becomes possible to identify microcircuits with internal defects of the "open" type.

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